HARRIS

IRFP450/451/452/453
IRFP450R/451R/452R/453R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 12A and 14A, 450V - 500V
- $r_{DS(on)}$ = 0.4Ω and 0.5Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

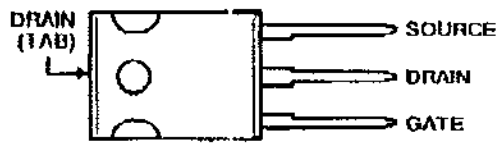
Description

The IRFP450, IRFP451, IRFP452, and IRFP453 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFP450R, IRFP451R, IRFP452R and IRFP453R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP types are supplied in the JEDEC TO-247 plastic package.

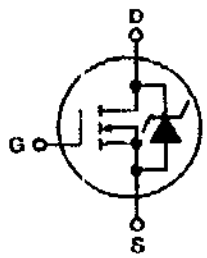
Package

TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

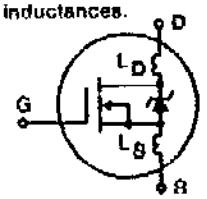
	IRFP450 IRFP450R	IRFP451 IRFP451R	IRFP452 IRFP452R	IRFP453 IRFP453R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	500	450	500	450	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	500	450	500	450	V
Continuous Drain Current					
T_C = +25°C ..... I_D	14	14	12	12	A
T_C = +100°C ..... I_D	8.8	8.8	7.9	7.9	A
Pulsed Drain Current (3) ..... I_{DM}	56	56	48	48	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	180	180	180	180	W
Linear Derating Factor	1.44	1.44	1.44	1.44	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	52	52	48	48	A
Single Pulse Avalanche Energy Rating (4) ..... E_{AS}*	860	860	860	860	mJ
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

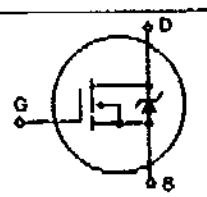
1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
   *R Suffix Types Only
4. V_{DD} = 50V, starting T_J = +25°C, L = 7.9mH, R_{GS} = 25Ω, I_{PEAK} = 14A. See Figure 15.

File Number 2331.1

Electrical Characteristics T_C = 25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFP450/452, IRFP450R/452R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	500	-	-	V
IRFP451/453, IRFP451R/453R			450	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_J = +125°C	-	-	1000	µA
On-State Drain Current (Note 2) IRFP450/451, IRFP450R/451R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	14	-	-	A
IRFP452/453, IRFP452R/453R			12	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFP450/451, IRFP450R/451R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 7.8A	-	0.3	0.4	Ω
IRFP452/453, IRFP452R/453R			-	0.4	0.5	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} ≥ 50V, I_D = 7.8A	9.3	13.8	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 10	-	2000	-	pF
Output Capacitance	C_{OSS}		-	400	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	100	-	pF
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 250V, I_D = 14A, R_G = 6.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	16	27	ns
Rise Time	t_r		-	45	68	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	68	100	ns
Fall Time	t_f		-	41	60	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 14A, V_{DS} = 0.8V Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	82	130	nC
Gate-Source Charge	Q_{gs}		-	12	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	42	-	nC
Internal Drain Inductance	L_D	Measured between the contact screw on header that is closer to source and gate pins and center of center of die. Modified MOSFET symbol showing the internal device inductances. 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from header and source bonding pad.	-	12.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	0.70	°C/W
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	0.10	-	°C/W
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	30	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	14	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	56	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 14A, V_{GS} = 0V	-	-	1.4	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 13A, dI_F/dt = 100A/µs	-	1300	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 13A, dI_F/dt = 100A/µs	-	7.4	-	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES: 1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. V_{DD} = 50V, Start T_J = +25°C, L = 7.8mH, R_G = 25Ω, I_{PEAK} = 14A (See Figure 15)

Performance Curves

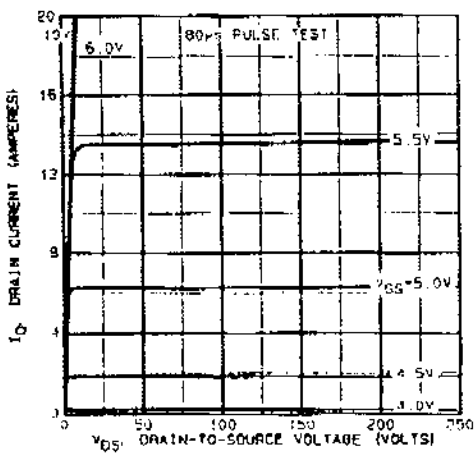


FIGURE 1. TYPICAL OUTPUT CHARACTERISTICS

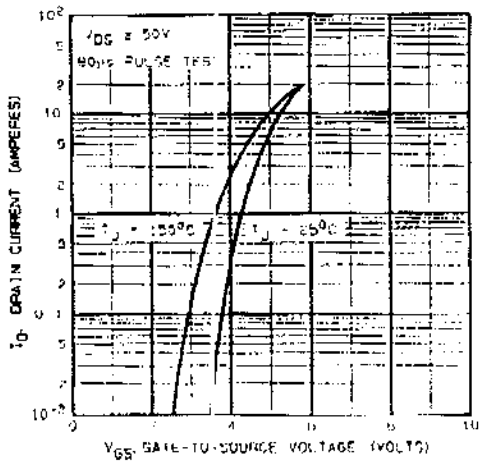


FIGURE 2. TYPICAL TRANSFER CHARACTERISTICS

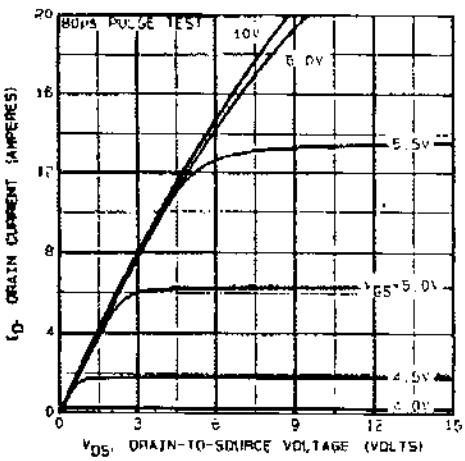


FIGURE 3. TYPICAL SATURATION CHARACTERISTICS

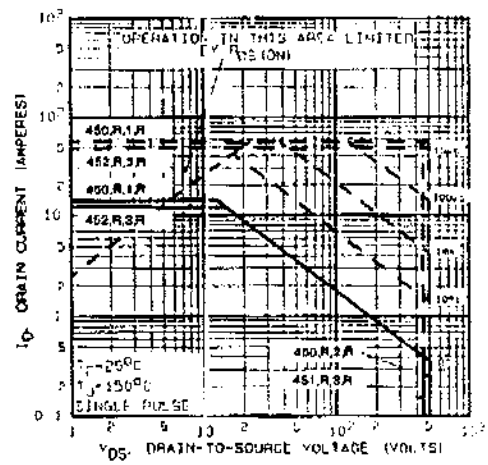


FIGURE 4. MAXIMUM SAFE OPERATING AREA

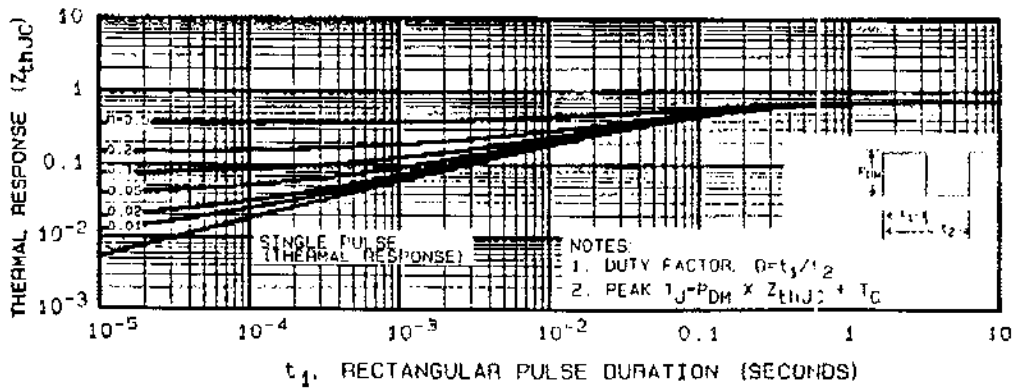


FIGURE 5. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

Performance Curves (Continued)

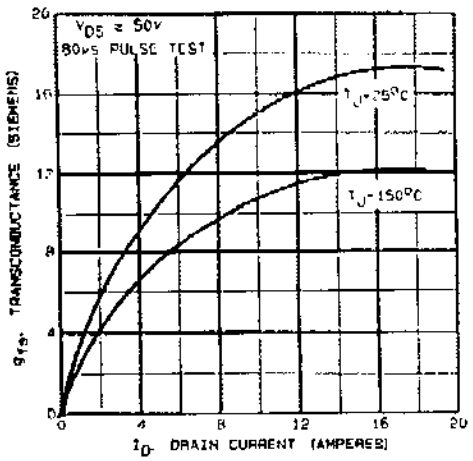


FIGURE 6. TYPICAL TRANSCONDUCTANCE vs DRAIN CURRENT

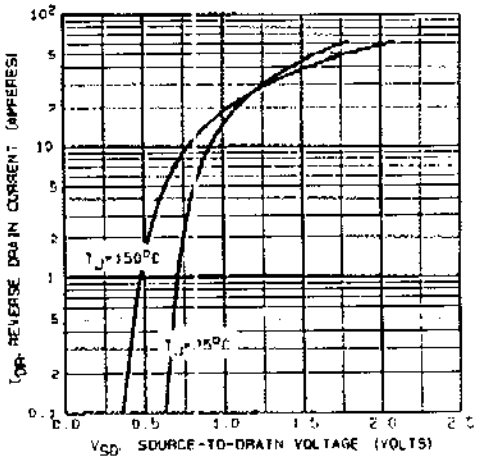


FIGURE 7. TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

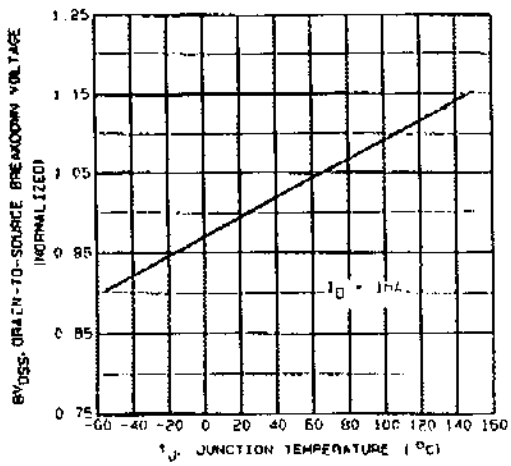


FIGURE 8. BREAKDOWN VOLTAGE vs TEMPERATURE

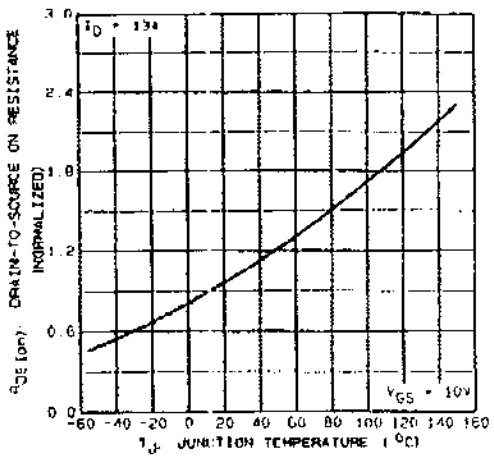


FIGURE 9. NORMALIZED ON-RESISTANCE vs TEMPERATURE

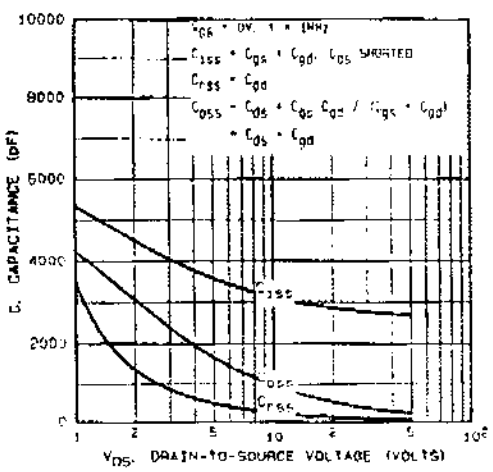


FIGURE 10. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

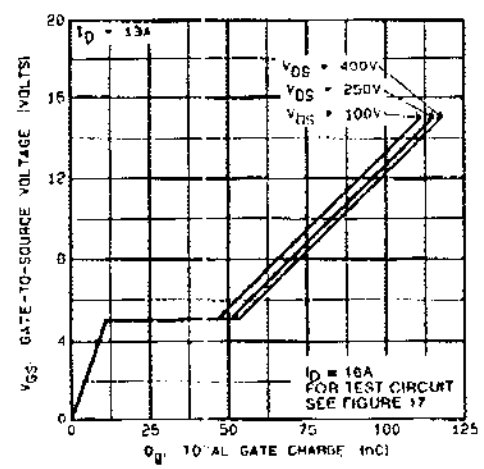


FIGURE 11. TYPICAL GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

Performance Curves (Continued)

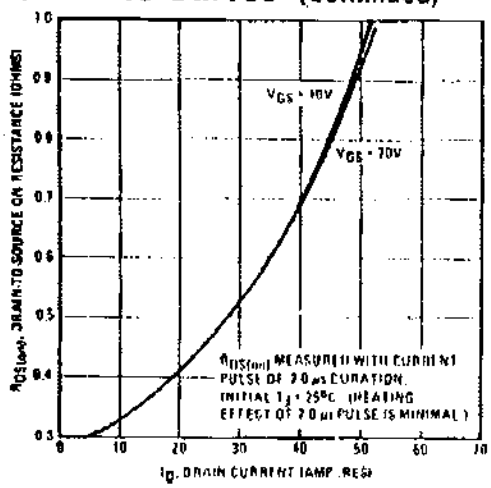


FIGURE 12. TYPICAL ON-RESISTANCE VS. DRAIN CURRENT

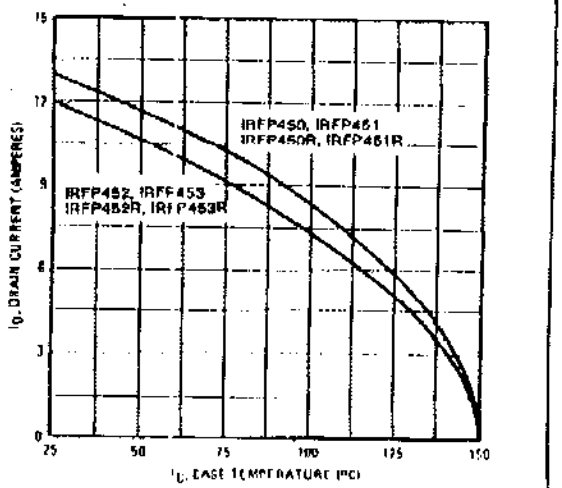


FIGURE 13. MAXIMUM DRAIN CURRENT VS. CASE TEMPERATURE

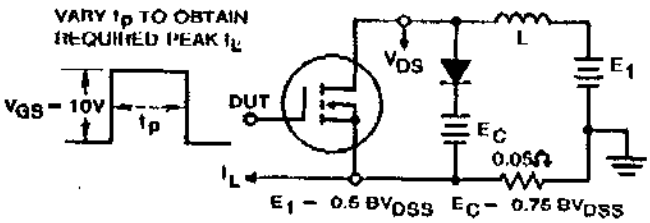


FIGURE 14a. CLAMPED INDUCTIVE TEST CIRCUIT

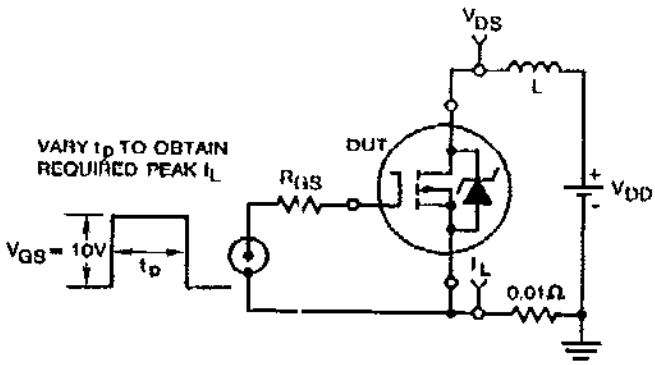


FIGURE 15a. UNCLAMPED ENERGY TEST CIRCUIT

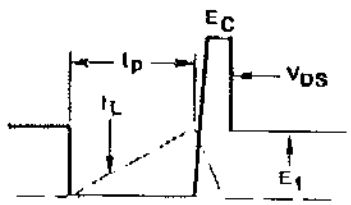


FIGURE 14b. CLAMPED INDUCTIVE WAVEFORMS

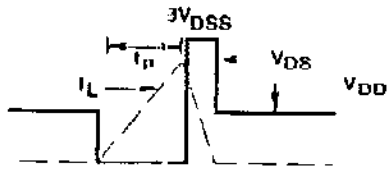


FIGURE 15b. UNCLAMPED ENERGY WAVEFORMS

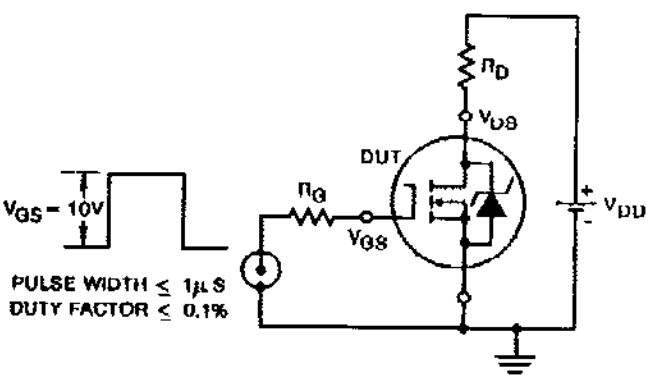


FIGURE 16. SWITCHING TIME TEST CIRCUIT

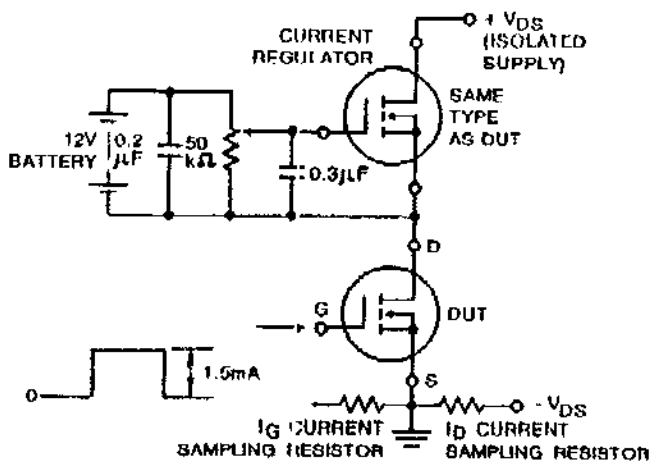


FIGURE 17. GATE CHARGE TEST CIRCUIT